Read Noise

Understanding sCMOS Read Noise

New sCMOS technology boasts an ultra-low read noise floor that significantly exceeds that which has been available from even the best CCDs, and at several orders of magnitude faster pixel readout speeds. For those more accustomed to dealing with CCDs, it is useful to gain an understanding of the nature of read noise distribution in CMOS imaging sensors.

Read Noise
CCD architecture is such that the charge from each pixel is transferred through a common readout structure, at least in single output port CCDs, where charge is converted to voltage and amplified prior to digitization in the Analogue to Digital Converter (ADC) of the camera. This results in each pixel being subject to the same readout noise. However, CMOS technology differs in that each individual pixel possesses its own readout structure for converting charge to voltage. In the CIS 2051 sCMOS sensor, each column possesses dual amplifiers and ADCs at both top and bottom (facilitating the split sensor readout). During readout, voltage information from each pixel is directly communicated to the appropriate amplifier/ADC, a row of pixels at a time; see tech note on Rolling and Global Shutter modes.

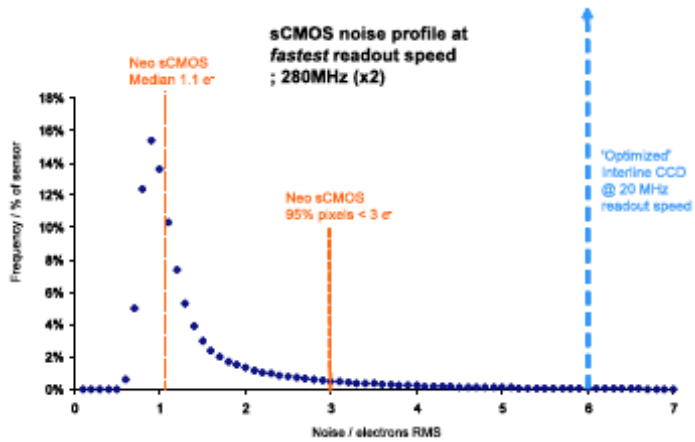

Figure 1 - Representative histogram showing read noise distribution at fastest readout speed of 560 MHz. The median value of 1.1 e- means 50% pixels have less than 1 e- and 50% have greater than 1 e-. The line at 6 e- represents a typical read noise value from a well optimized Interline CCD - all pixels in a CCD share the same noise value.

As a consequence of each pixel having its own individual readout structure, the overall readout noise in CMOS sensors is described as a distribution, as exemplified in figure 1, which is a representative noise histogram from a Neo sCMOS camera at the fastest readout speed of 560 MHz (or 280 MHz x 2). It is standard to describe noise in CMOS technology by citing the median value of the distribution. In the data presented, the median value is 1.1 electron rms. This means that 50% of pixels have a noise less than 1.1 electrons, and 50% have noise greater than 1.1 electrons. While there will be a small percentage of pixels with noise greater than 2 or 3 electrons, observable as the low level tail towards the higher noise side of the histogram, it must be remembered that a CCD Interline camera reading out at 20 MHz would have 100% of its pixels reading out with read noise typically ranging between 6 and 10 electrons rms (depending on camera manufacture).

Insight into the sCMOS architecture The sensor features a split readout scheme in which the top and bottom halves of the sensor are read out independently. Each column within each half of the sensor is equipped with dual column level amplifiers and dual analog-to-digital converters (ADC); see technical note of Dual Column Amplifiers for more detail. This 'split' sensor format was designed to help minimize read noise while maintaining extremely fast frame rates. Each pinned-photodiode pixel has 5 transistors ('5T' design), enabling the novel 'global shutter' mode and also facilitating correlated double sampling (CDS), to further reduce noise, and a lateral anti-blooming drain. The sensor is integrated with a microlens array that serves to focus much of the incident light per pixel away from the transistors and onto the exposed silicon, enhancing the QE (analogous to use of microlenses in Interline CCDs to focus light away from the column masks).

The sensor is configured to offer low dark current and extremely low read noise with true CDS. Non-linearity is less than 1% and is further correctable to < 0.2%. The sensor also has anti-blooming of >10,000:1, meaning that the pixels can be significantly oversaturated without charge spilling into neighboring pixels. It is also possible to use the anti-blooming capability to hold all or parts of the sensor in a state of 'reset', even while light is falling on these pixels.

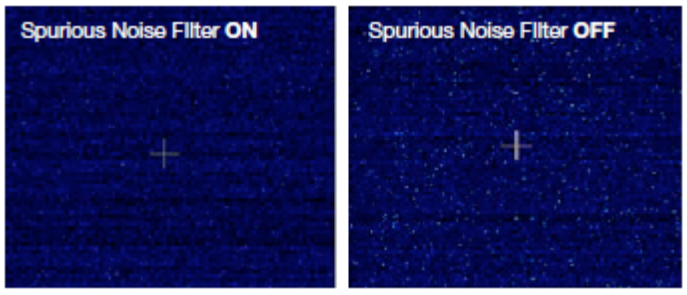

Figure 2 - Demonstration of Spurious Noise Filter on a dark image, 20 ms exposure time, 200 MHz (x2) readout speed (~ 1.2 e- readnoise)

Spurious Noise Filter Andor's Neo sCMOS camera comes equipped with an optional in-built FPGA filter to reduce the frequency of occurrence of high noise pixels. This real time filter corrects for pixels that are above 5 electrons rms and would otherwise appear as spurious 'salt and pepper' noise spikes in the image. The appearance of such noisy pixels is analogous to the situation of Clock Induced Charge (CIC) noise spikes in EMCCD cameras, in that it is due to the fact that we have significantly reduced the noise in the bulk of the sensor, such that the remaining small percentage of spuriously high noise pixels can become an aesthetic issue. The filter employed dynamically identifies such high noise pixels and replaces them with the mean value of the neighbouring pixels.